REMARKS

The application includes claims 1-15, 17-23, and 25-28 prior to entering this amendment.

The examiner rejects claims 1-12 and 28 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

The examiner rejects claims 11-13, 22, 23, and 28 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

The examiner rejects claims 1-15, 17-23, and 25-28 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the applicants regard as their invention.

The examiner rejects claims 1, 2, 5-9, 11, and 12 under 35 U.S.C. § 102(e) as being anticipated by Arora et al. (U.S. Patent 6,625,693), as cited in the previous office action.

The examiner rejects claims 1-4 under 35 U.S.C. § 102(c) as being anticipated by Crump et al. (U.S. Patent 5,557,759), as cited in the previous office action.

The applicants amend claims 1, 4, 10-14, 22, 25-28. The applicants cancel claims 2-3. The applicants had previously canceled claims 16 and 24.

The application remains with claims 1, 4-15, 17-23, and 25-28 after entering this amendment.

The applicants add no new matter and request reconsideration.

Claim Rejections Under § 112

The examiner rejects claim 1-12, and 28 as failing to adequately describe the limitation *concurrently in-line staging*. Although the applicants disagree with the examiner that the limitation is not adequately described in the specification, they nonetheless amend the claims to remove the claim and further prosecution.

The examiner rejects claims 11-13, 22, 23, and 28 as failing to adequately teach how to insert or retire micro-opcodes into an instruction cache. The applicants traverse the rejections for the reasons that follow.

The specification well enables how to insert and/or retire instructions. For example, the specification at page 6, describes that the out-of-order execution unit 24 "schedules and executes the μOPs stored in the ROB that is loaded by p-code decoder 18. A reservation station (RS)

within out-of-order execution unit 24 continuously scans the ROB for μOPs that are ready to be executed and dispatches them to one or more of five execution ports.... Instruction retirement unit 26 simply stores the executed instructions from OOO execution unit 24, in their original consecutive order, into instruction cache 22 for future re-use by instruction fetch unit 20. Those of skill in the art will appreciate that instruction retirement ensures that instruction cache 22 thus will contain instructions that may be required by instruction fetch unit 20 when instruction fetch unit 20 performs its next instruction pre-fetch. This avoids the latencies related to memory bus contention and read access that otherwise would slow processing if the same instruction sequence is required to be performed again, as may often be the case."

The examiner rejects claims 1-15, 17-23, and 25-28 as being indefinite. The applicants traverse the rejection for the reasons that follow.

The examiner indicates the term concurrently in-line staging is unclear. The applicants have amended the claims to obviate the rejection.

The examiner rejects claim 14 for not being clear whether the instruction queue mechanism contains instructions or p-code.

The applicants amend claim 14 such that the instruction queue mechanism stages instruction for decoding by a p-code decoder. Referring to Fig. 1, the instruction fetch unit 20 and the instruction cache unit 20 forms the instruction queue mechanism, indicated at 28. The instruction fetch unit 20 stages instructions from decoding by p-code decoder 18 to which its output instruction stream is routed.[1]

The examiner rejects claim 22 for not being clear and confusing phrase such as instruction sequence or stream and p-code sequence and stream.

The applicants amend claim 22 to clarify the confusion. As for the meaning of "predicated on an instruction stream," p-code decoder 18 shown in figure 3B includes a state machine that includes a context switch prediction unit that predicts naturally occurring context switches in anticipation thereof. "Such predictions are predicated on the routine, i.e., interrupt independent, instruction stream, that most recently was decoded by p-code decoder 18 for dispatch and execution by OOO execution unit 24."[2]

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[1] Specification, page 6, lines 13-15.

[2] Specification, page 16, lines 10-17.

The examiner rejects claim 25 for lacking proper antecedent basis for the interrupt service instructions and the "to insert into an instruction sequence decoded micro-opcodes."

The applicants amend claim 25 to provide proper antecedent basis and obviate the examiner's rejection. The applicants further amend claim 15 to require that an interrupt-handler instructs the fetch and decode units to insert into an instruction sequence decoded micro-ops representing interrupt servicing instructions for scheduling and execution by the dispatch and execute units, *wherein the instruction sequence also comprises decoded micro-ops representing other program instructions*. Therefore an instruction sequence recited in claim 25 is a sequence of decoded micro-ops, including micro-ops representing interrupt servicing instructions and micro-ops representing other program instructions.

The examiner rejects claim 28 for confusing terms "micro-ops" and "micro-opcodes," and for not being clear whether the retiring is done to an instruction queue mechanism or to an instruction cache.

The applicants amend claim 28 to replace micro-opcodes with micro-ops. The applicants would like to clarify that retiring is done to an instruction cache. This statement is supported by claim 28, which recites *retiring the executed micro-op ... to an instruction cache*.[3]

Independent claims 10, 13, 14, 22, 25, and 28 and their corresponding dependent claims 15, 17-21, 23, and 26-27 are in condition for the examiner's allowance.

Claim Rejections Under § 102

The examiner alleges claims 1-2, 5-9, and 11-12 are old over Arora. And the examiner alleges claims 1-4 are old over Crump. The applicants traverse the examiner's rejections for the reasons that follow.

The applicants amend claim 1 to include the limitations of now canceled claims 2 and 3. Claim 1 now recites *recycling the executed micro-ops for optional re-execution in the one or more out-of-order execution units by retiring the executed micro-ops including those micro-ops representing the inserted interrupt servicing instructions to the instruction cache*. Claim 11 includes a similar retirement unit.

[3] Specification, page 6, lines 19-21.

The examiner does not reject claim 3 over Arora, tacitly acknowledging that Arora does not disclose the recycling limitation now included in claim 1. Rather, Arora teaches a fast exception processing system, which includes a splice cache, an exception logic, and an instrumentation mechanism.

The examiner alleges that Crump teaches concurrently in-line staging the ISR instruction after mainstream instructions. But Crump does not teach inserting interrupt servicing instructions into mainline program instruction within an instruction queue such that a processor can process the interrupt servicing instruction concurrently with the mainline program instructions as recited. Crump indicates that the interrupt servicing instruction is not executed concurrently with the mainline codes. Rather when the interrupt occurs, the mainline program is stalled and the program counter is stored in the BAL1 and the interrupt counter is loaded.[4] Crump's instruction cache is time-shared between mainline codes, interrupt requests.[5]

As such, independent claims 1 and 11 and their corresponding dependent claims 4-9 and 12 are in condition for allowance.

Conclusion

For the foregoing reasons, the applicants request reconsideration and allowance of all remaining claims. The applicants encourage the examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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[4] Crump, column 18, lines 25-28.
[5] Crump, column 18, lines 35-36.